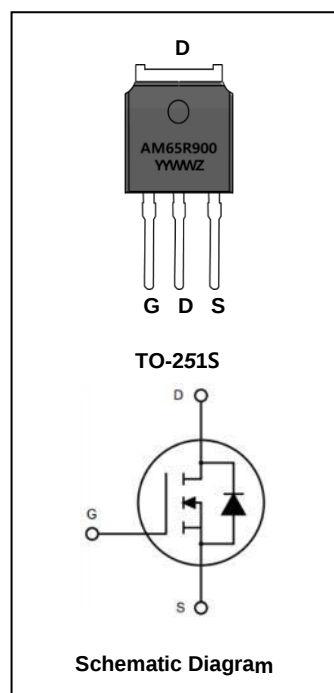


Main Product Characteristics:

$V_{(BR)DSS}$	650V
$R_{DS(ON)}$	0.78Ω(typ.)
I_D	5A

Features and Benefits

- Grand Turbo MOSFET process technology.
- Optimized the cell structure.
- Low on-resistance and low gate charge.
- Featuring low switching and drive losses.
- Fast switching and reverse body recovery.
- High ruggedness and robustness.



Description

The Grand Turbo MOSFET series products utilize outstanding standard turbo process and packaging techniques to achieve ultra-low on-resistance and low gate charge and to provide the industry's best-in-class performance.

These features make this series products extremely efficient, temperature characteristics and reliable for use in power management, synchronous rectification, battery protection, load switch and a wide variety of other applications.

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Parameter.	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-to-Source Voltage	V_{GS}	±30	V
Continuous Drain Current, @ Steady-State	$I_D @ T_C = 25^\circ\text{C}$	5	A
Continuous Drain Current, @ Steady-State	$I_D @ T_C = 100^\circ\text{C}$	3.2	A
Pulsed Drain Current	I_{DM}	20	A
Power Dissipation	$PD @ T_C = 25^\circ\text{C}$	42	W
		0.34	W/°C
Single Pulse Avalanche Energy ¹	E_{AS}	214	mJ
Single Pulse Avalanche Current	I_{AS}	2.8	A
Body diode reverse voltage slope ²	dv/dt	15	V/ns
MOS dv/dt reggedness ³	dv/dt	50	V/ns
Junction-to-Ambient (PCB Mounted, Steady-State)	$R_{\theta JA}$	62.0	°C/W
Junction-to-Case	$R_{\theta JC}$	2.97	°C/W
Operating Junction and Storage Temperature Range	T_J/T_{STG}	-55 to + 150	°C
Soldering temperature	T_{sold}	260	°C

Electrical Characteristics (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	650	-	-	V
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V, T _J =25°C	-	-	1.0	μA
		V _{DS} =650V, V _{GS} =0V, T _J =125°C	-	1.5	-	μA
Gate-to-Source Forward Leakage	I _{GSS}	V _{DS} =0V, V _{GS} =30V	-	-	100	nA
		V _{DS} =0V, V _{GS} = -30V	-	-	-100	
Static Drain-to-Source On- Resistance	R _{DS(on)}	V _{GS} =10V, I _D =2.5A	-	0.78	0.90	Ω
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	-	4.0	V
Gate Resistance	R _g	f=1MHz	-	7.2	-	Ω
Input Capacitance	C _{iss}	V _{GS} =0V V _{DS} =100V, f=1MHz	-	300	-	pF
Output Capacitance	C _{oss}		-	20	-	
Reverse transfer capacitance	C _{rss}		-	2.4	-	
Total Gate Charge ^{4,5}	Q _g	I _D =5A, V _{DD} =520V, V _{GS} =10V	-	13	-	nC
Gate-to-Source Charge ^{4,5}	Q _{gs}		-	3.0	-	
Gate-to-Drain("Miller") Charge ^{4,5}	Q _{gd}		-	6.8	-	
Gate Plateau ^{4,5}	V _{plateau}		-	6.5	-	V
Turn-on Delay Time ^{4,5}	t _{d(on)}	V _{DD} =325V, V _{GS} =10V, R _G =24Ω, I _D =5A	-	8.7	-	nS
Rise Time ^{4,5}	t _r		-	25	-	
Turn-Off Delay Time ^{4,5}	t _{d(off)}		-	30	-	
Fall Time ^{4,5}	t _f		-	23	-	

Source-Drain Ratings and Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Continuous Source Current (Body Diode)	I _S	T _C =25°C, MOSFET symbol showing the integral reverse p-n junction diode.	-	-	5	A
Diode Pulse Current	I _{S,pulse}		-	-	20	A
Diode Forward Voltage	V _{SD}	I _S =5A, V _{GS} =0V	-	-	1.4	V
Reverse Recovery Time ⁴	t _{rr}	I _S =5A, V _{GS} =0V, dI _F /dt=100A/us	-	334	-	nS
Reverse Recovery Charge ⁴	Q _{rr}		-	2.2	-	μC

Notes:

1. L=79mH, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C.
2. V_{DS}=0~400V, I_{SD}≤I_S, T_J=25°C.
3. V_{DS}=0~480V.
4. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
5. Essentially Independent of Operating Temperature.



Typical Electrical and Thermal Characteristic Curves

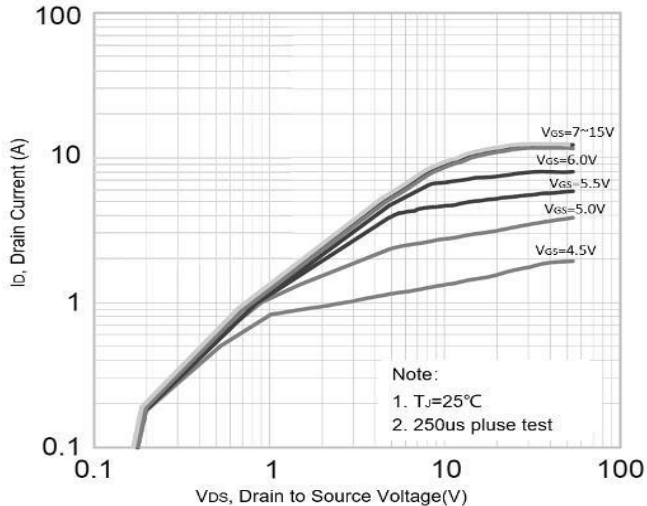


Figure1. Typical Output Characteristics

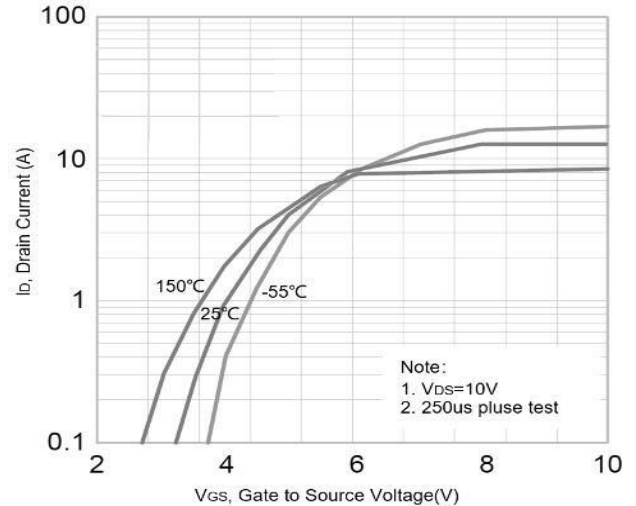


Figure2. Transfer Characteristics

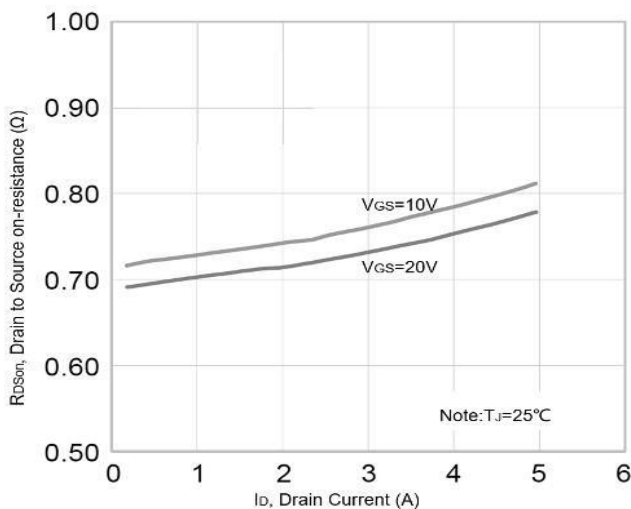


Figure3. $R_{DS(on)}$ vs. Drain Current

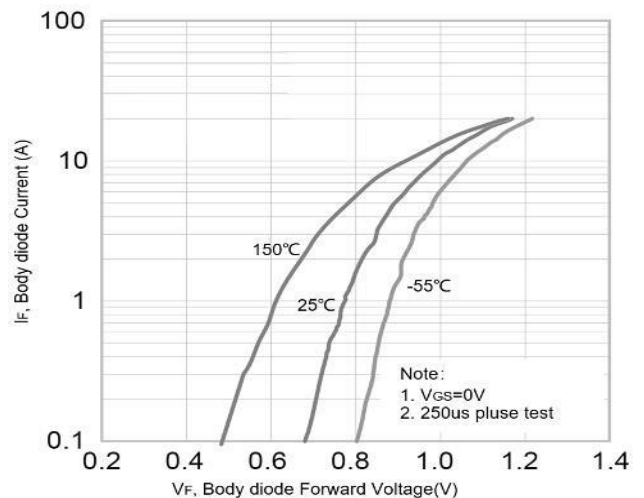


Figure4. Body Diode Characteristic

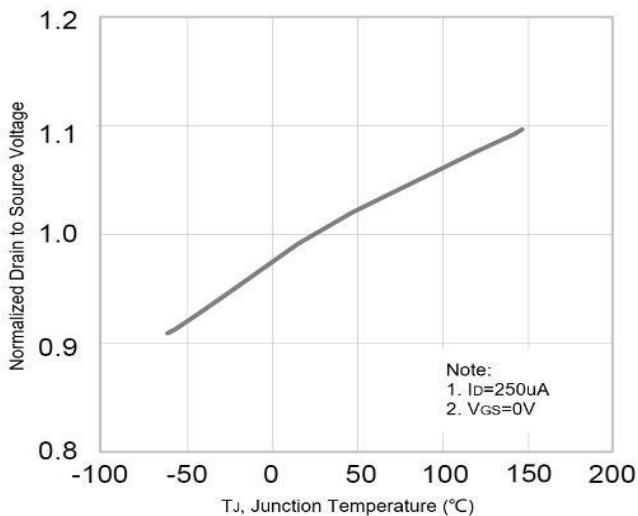


Figure5. Normalized BV_{DSS} vs. T_J

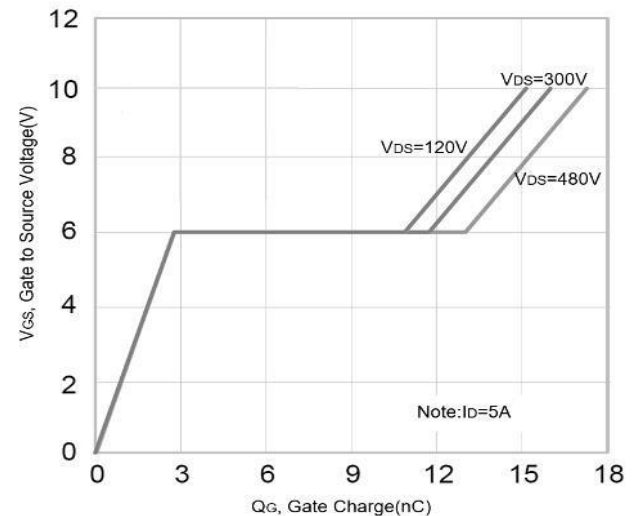


Figure6. Gate Charge Characteristic



Typical Electrical and Thermal Characteristic Curves

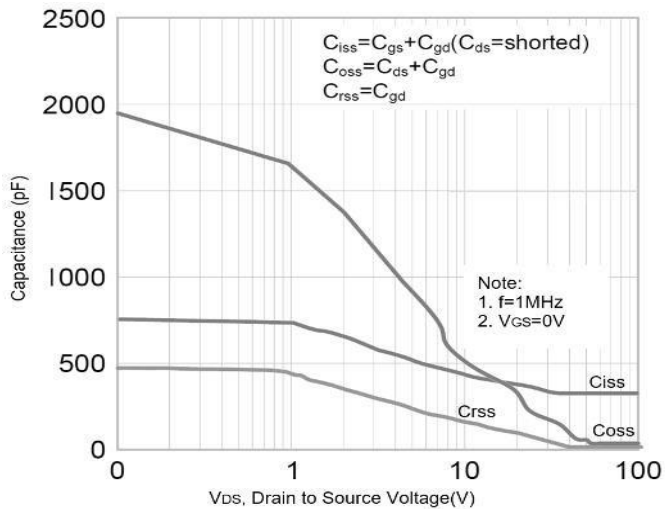


Figure7 Capacitance Characteristic

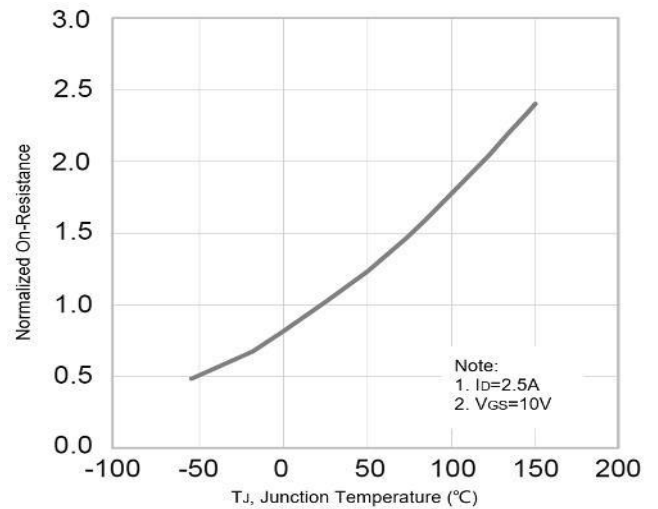


Figure8 Normalized Rdson vs.T_j

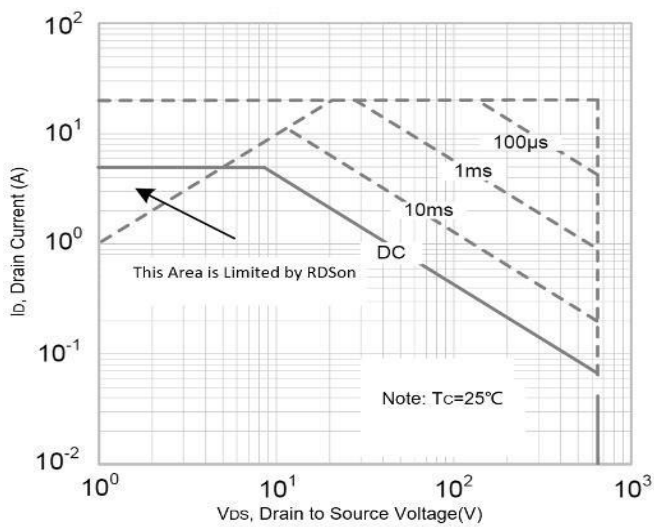


Figure9. Safe Operation Area

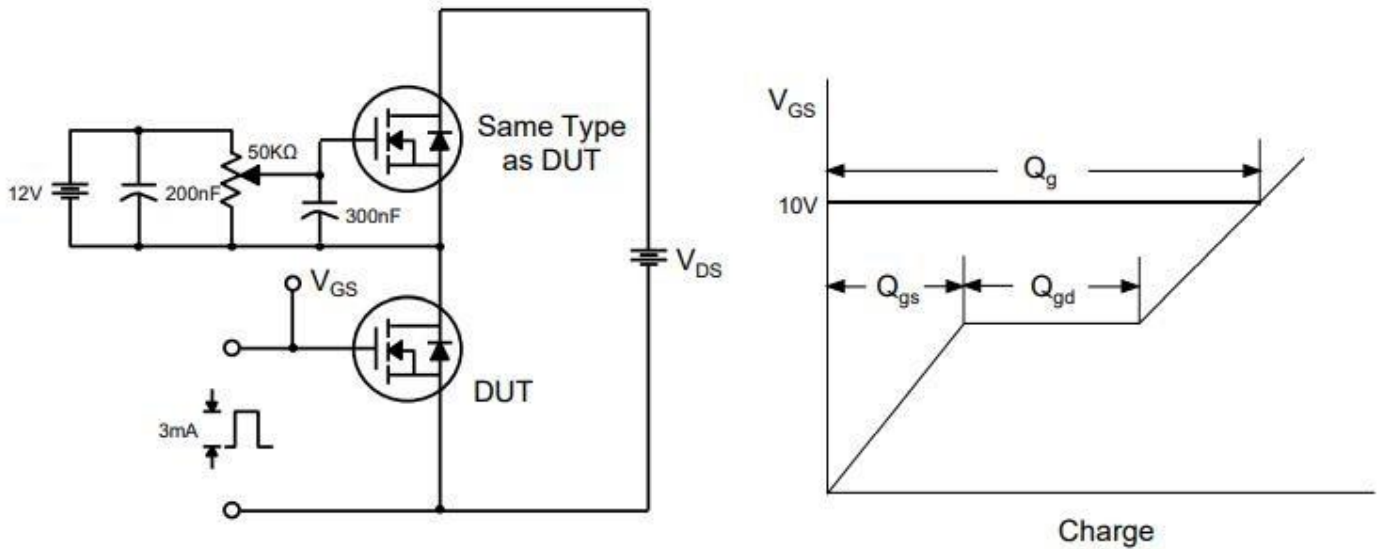


Figure 10. Gate Charge Test Circuit & Waveforms

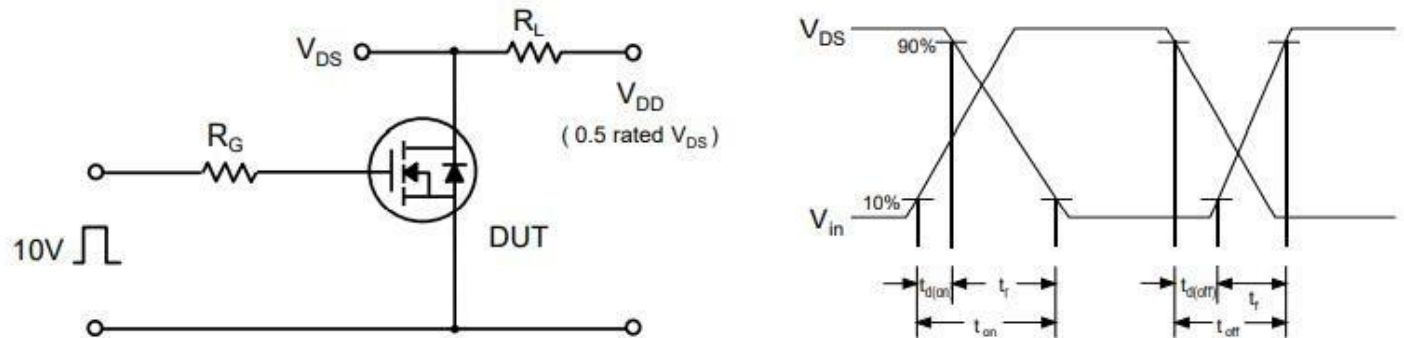


Figure 11. Resistive Switching Test Circuit & Waveforms

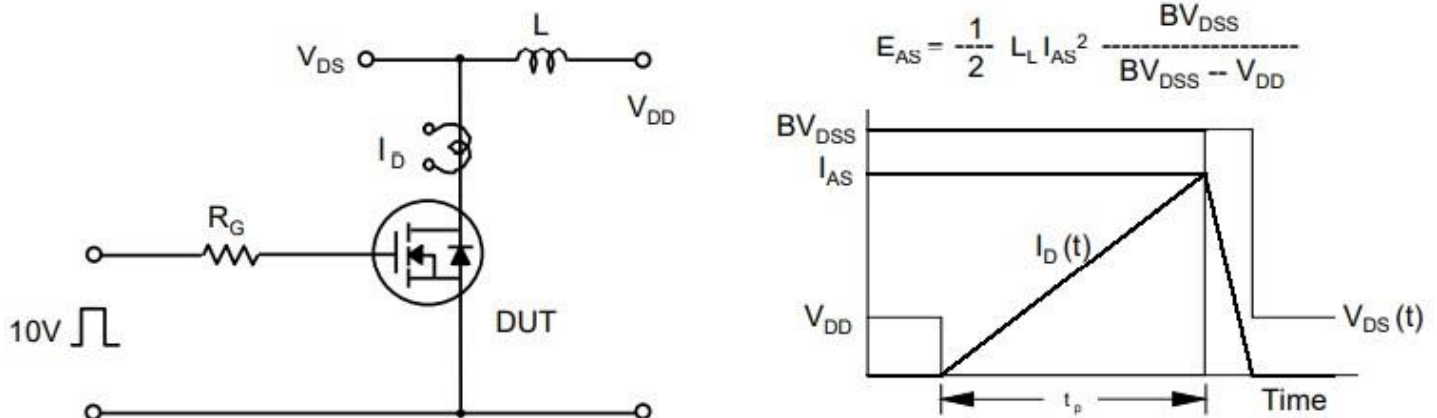
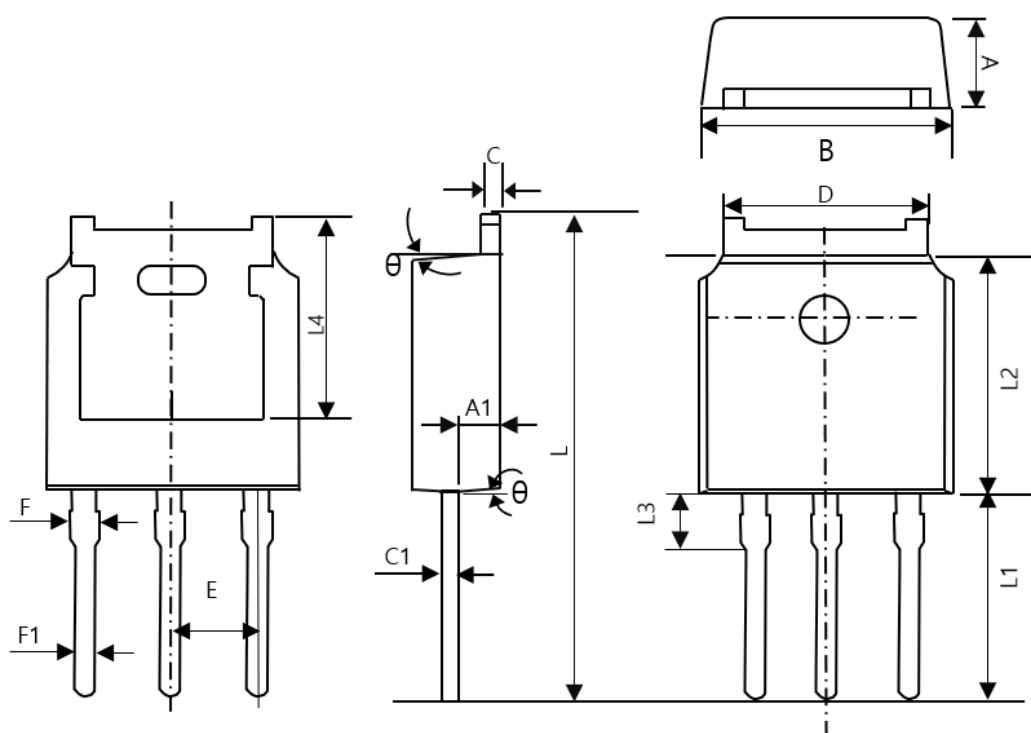


Figure 12. Unclamped Inductive Switching Test Circuit & Waveforms



Package Outline Dimensions

TO-251-3L



TO-251S-3L		unit : mm	
DIM	MIN	NOM	MAX
A	2.25	2.3	2.35
A1	0.91	1.01	1.11
B	6.50	6.6	6.70
C	0.46	0.52	0.58
C1	0.46	0.52	0.58
D	5.1	5.28	5.46
E	2.186	2.286	2.386
F	0.74	0.84	0.94
F1	0.66	0.76	0.86
L	11.70	12.00	12.30
L1	4.8	5.0	5.2
L2	6.0	6.1	6.2
L3	1.12	1.13	1.14
L4		5.2	
θ		7° REF	



Revision History

No	Date	Contents
0	2023-03-20	Initial Brief Datasheet Release

<http://www.apsemi.com>

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